

Appl. No. 10/808,802  
Amdt. dated 3/21/05  
Reply to Office Action of 01/21/2005

Attorney Docket No.: TS03-186  
N1085-90102

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

- 1        1. (Currently Amended) A method of forming an opening in a stack of insulator layers, comprising the steps of:
  - 3            providing a conductive structure;
  - 4            forming said stack of insulator layer layers on said conductive structure, with said stack of insulator layers comprised of [[an]] a first liner layer, an overlying first insulator layer, a second liner layer, an overlying second insulator layer, an anti-reflective coating (ARC), layer; and a capping, third insulator layer;
  - 8            forming a via opening in a first portion of said stack of insulator layer, with said via opening extending downwardly from a top surface of said capping, third insulator layer and terminating in said first liner layer;
  - 11          forming a photoresist shape including a trench-defining shape and a photoresist plug that completely fills said via opening up to said top surface, said trench-defining shape exposing a second portion of said stack of insulator layers;
  - 14          forming a trench opening in [[a]] said second portion of said stack of insulator layers using said trench-defining shape as an etch mask, with said trench opening extending downwardly from a top surface of said capping, third insulator layer and terminating on top surface of said second liner layer,
  - 18          removing portion of said second liner layer exposed in said trench opening;
  - 19          removing said photoresist shape including said photoresist [[plus]] plug; and
  - 20          removing a portion of said first liner layer exposed in said via opening, exposing a portion of a top surface of said conductive structure.

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1           2. (Original) The method of claim 1, wherein said conductive structure is  
2 comprise of copper.

1           3. (Original) The method of claim 1, wherein said first liner is a silicon nitride  
2 layer, obtained via plasma enhanced chemical vapor deposition (PECVD) procedures at  
3 a thickness between about 400 to 600 Angstroms.

1           4. (Original) The method of claim 1, wherein said first insulator layer is a  
2 fluorinated silica glass (FSG) layer, obtained via PECVD procedures at a thickness  
3 between about 500 to 1000 Angstroms.

1           5. (Original) The method of claim 1, wherein said second liner layer is a  
2 silicon nitride layer, obtained via PECVD procedures at a thickness between about 200  
3 to 400 Angstroms.

1           6. (Original) The method of claim 1, wherein said second insulator layer is a  
2 silicon oxide layer, obtained via PECVD procedures at a thickness between about 500  
3 to 1000 Angstroms.

1           7. (Original) The method of claim 1, wherein said ARC layer is a silicon  
2 oxynitride layer, obtained via PRCVD procedures to a thickness between about 500 to  
3 700 Angstroms.

1           8. (Original) The method of claim 1, wherein said capping, third insulator  
2 layer is a silicon oxide layer, obtained via PECVD procedures at a thickness between  
3 about 500 to 700 Angstroms.

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1           9. (Original) The method of claim 1, wherein said via opening is defined in  
2 said capping, third insulator layer, in said ARC layer, in said second insulator layer, in  
3 said second liner layer, and in said first insulator layer, via an anisotropic reactive ion  
4 etching (RIE) procedure, using  $\text{CHF}_3$  as an etchant for said capping, third insulator  
5 layer, for said second insulator layer, for said ARC layer and for said first insulator layer,  
6 while  $\text{CH}_x\text{F}_y$  or  $\text{CF}_4$  is used as an etchant for said second liner layer.

1           10. (Original) The method of claim 1, wherein the diameter of said via  
2 opening is between about 0.25 to 2.5  $\mu\text{m}$ .

1           11. (Original) The method of claim 1, wherein said trench opening is defined  
2 in said capping, third insulator layer, in said ARC layer, and in second insulator layer via  
3 an anisotropic RIE procedure using  $\text{CHF}_3$  as an etchant.

1           12. (Original) The method of claim 1, wherein portion of said second liner  
2 layer exposed in said trench opening, is removed via a selective RIE procedure using  
3  $\text{CF}_4$  or  $\text{CH}_x\text{F}_y$  as an etchant.

1           13. (Previously Presented) The method of claim 1, wherein said photoresist  
2 shape is removed using plasma oxygen ashing procedures.

1           14. (Original) The method of claim 1, wherein portion of said first liner layer  
2 exposed in said via opening, is removed via a selective RIE procedure using  $\text{CF}_4$  or  
3  $\text{CH}_x\text{F}_y$  as an etchant.

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1        15. (Original) The method of claim 1, wherein the etch rate ratio of silicon  
2        nitride of said first liner layer, to silicon oxide, during the selective RIE procedure used  
3        to remove portion of said first liner layer exposed in said via opening, is between about  
4        5 to 1, to 10 to 1 using CF<sub>4</sub> or CH<sub>x</sub>F<sub>y</sub> as an etchant.

1        16. (Currently Amended) A method of forming a dual damascene opening in  
2        a stack of insulator layers featuring a two step stop layer removal procedure, comprising  
3        the steps of:

4            providing a copper structure;

5            forming said stack of insulator layers on said copper structure, with said stack of  
6        insulator layers comprised of an underlying first silicon nitride stop layer, an overlying  
7        first dielectric layer, a second silicon nitride stop layer, a second dielectric layer, an anti-  
8        reflective coating (ARC) layer, and a capping silicon oxide layer;

9            forming a via opening in a first portion of said stack of insulator layer, with said  
10      via opening extending downwardly from a top surface of said capping silicon oxide layer  
11      and terminating in said first silicon nitride stop layer;

12           forming a photoresist shape including a trench-defining shape and a photoresist  
13      plug that completely fills said via opening up to said top surface and overlies a portion of  
14      a surface of said first silicon nitride layer, said trench-defining shape exposing a second  
15      portion of said stack of insulator layers;

16           forming etching to form a trench opening in [[a]] said second portion of said stack  
17      of insulator layers using said trench-defining shape as an etch mask, with said trench  
18      opening extending downwardly from a top surface of said capping silicon oxide layer  
19      and terminating on said surface of said second silicon nitride stop layer;

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20 performing a first step of said two step stop layer removal procedure to  
21 selectively remove a portion of said second silicon nitride stop layer exposed in said  
22 trench opening;

23 removing said photoresist shape including said photoresist plug; and

24 performing a second step of said two step stop layer removal procedure to  
25 remove a portion of said first silicon nitride stop layer exposed in said via opening,  
26 exposing a portion of a top surface of said copper structure.

1 17. (Original) The method of claim 16, wherein said first silicon nitride stop  
2 layer is obtained via plasma enhanced chemical vapor deposition (PECVD) procedures  
3 at a thickness between about 400 to 600 Angstroms.

1 18. (Original) The method of claim 16, wherein said first dielectric layer is an  
2 FSG layer, obtained via PECVD procedures at a thickness between about 500 to 1000  
3 Angstroms.

1 19. (Original) The method of claim 16, wherein said second silicon nitride  
2 stop layer is obtained via PECVD procedures at a thickness between about 200 to 400  
3 Angstroms.

1 20. (Original) The method of claim 16, wherein said second dielectric layer is  
2 a silicon oxide layer, obtained via PECVD procedures at a thickness between about 500  
3 to 1000 Angstroms.

1 21. (Original) The method of claim 16, wherein said ARC layer is a silicon  
2 oxynitride layer, obtained via PECVD procedures to a thickness between about 500 to  
3 700 Angstroms.

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1        22. (Original) The method of claim 16, wherein said capping, silicon oxide  
2 layer is obtained via PECVD procedures at a thickness between about 500 to 700  
3 Angstroms.

1        23. (Original) The method of claim 16, wherein said via opening is defined in  
2 said capping silicon oxide layer, in said ARC layer, in said second dielectric layer, in  
3 said second silicon nitride stop layer, and in said first dielectric layer via an anisotropic  
4 reactive ion etching (RIE) procedure, using CHF<sub>3</sub> as an etchant for said capping silicon  
5 oxide layer, for said ARC layer and for said second dielectric layer and for said first  
6 dielectric layer, while CF<sub>4</sub> or CH<sub>x</sub>F<sub>y</sub> is used as an etchant for said second silicon nitride  
7 stop layer.

1        24. (Original) The method of claim 16, wherein the diameter of said via  
2 opening is between about 0.25 to 2.5 um.

1        25. (Original) The method of claim 16, wherein said trench opening is defined  
2 in said capping silicon oxide layer, in said ARC layer, and in said second dielectric layer,  
3 via an anisotropic RIE procedure using CHF<sub>3</sub> as an etchant.

1        26. (Original) The method of claim 16, wherein said first step of said two step  
2 stop layer removal procedure, used to selectively remove portion of said second silicon  
3 nitride stop layer exposed in said trench opening, is performed via a selective RIE  
4 procedure using CF<sub>4</sub> or CH<sub>x</sub>F<sub>y</sub> as an etchant.

1        27. (Previously Presented) The method of claim 16, wherein said photoresist  
2 shape is removed using plasma oxygen ashing procedures.

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1        28. (Original) The method of claim 16, wherein said second step of said two  
2        step stop layer removal procedure, used to selectively remove portion of said first silicon  
3        nitride stop layer exposed in said via opening, is performed via a selective RIE  
4        procedure using  $CF_4$  or  $CH_xF_y$  as an etchant.

1        29. (Original) The method of claim 16, wherein the etch ratio of silicon nitride  
2        to silicon oxide, during said second step of said two step stop layer removal procedure  
3        performed via a selective the selective RIE procedure used to remove portion of said  
4        first silicon nitride stop layer exposed in said via opening, is between about 5 to 1, to 10  
5        to 1 using  $CF_4$  or  $CH_xF_y$  as an etchant.